**North South University**

School of Engineering & Physical Sciences



Department of Electrical & Computer Engineering

**Project Report**

**Group-07**

Course Code: **CSE231**

Section: **06**

**Topic:** Display “CSE 231- 6” in a 7-segment display using a **Decoder.**

Name- **Shahrear Iqbal Nirzhor** ID- **1421717042**

Name- **Md Sharif Hossain**  ID- **1712336642**

Name- **Adiba Samreen Mahmud** ID**- 1711939642**

Name- **Rezuan Ahmed** ID**- 1620645042**

1. **Project Goal:** Display “CSE 231 - 6” in a 7-segment display using a **Decoder.**
2. **Equipment List:**

|  |  |
| --- | --- |
| **Name** | **Quantity** |
| 1. Trainer Board | 3 pieces |
| 1. Wires | 60 pieces |
| 1. 7-segment display | 1 piece |
| 1. 9 Volt Battery | 1 piece |
| 1. 9 Volt Battery Connector | 1 piece |
| 1. Voltage regulator   (9V to 5V) LM7805 | 1 piece |
| 1. IC 4075(3-input OR Gate) | 3 pieces |
| 1. IC 7432(Quad 2- input OR Gate) | 2 piece |
| 1. IC 74138(Decoder) | 1 piece |

1. **Theory**

Despite having several available options, we designed our circuit primarily focusing on a Decoder. Since, we believe, this process is very simple and cost efficient as well. In order to keep our circuit minimalistic and simple we used 1 Decoder (74138), 3 IC 4075 (3-input OR Gates) and 2 IC 7432 (2-input OR Gates).

**Decoders** are type of digital logic device. It can have 2-bit, 3-bit or 4-bit of input based the number of data input lines. If we have “n” number of input bits we can have 2n possible values. That means for 3 input bits we can have 23 i.e. 8 outputs. This is how, we can get a non- binary output from binary inputs.

* To make this circuit, we need to **3\*8** decoder. It takes three inputs and gives eight outputs.
* First, we need to make a truth table for the required circuit of the project using Decoder.
* After making circuit, we get seven equations from the truth table. Make sure about the findings equation that all the equations must be in **minterms** form.
* Then we understand what to do next for our project. How many IC’s and gates are needed can easily be found from the equation.
* Then we do circuit in logisim. According to our logisim circuit diagram, we can start our hardware implementation.

1. **Circuit Diagram:**

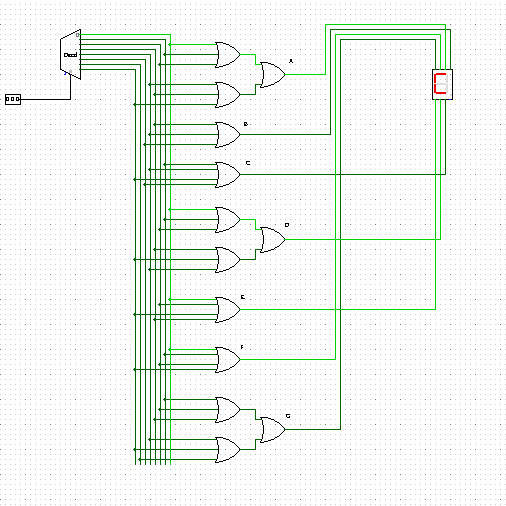
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Figure: logisim simulation for Decoder (Combinational)

1. **Implementation using other ways:**

**Using Basic Logic Gates:** For constructing the circuit using basic logic gates, a truth table followed with a simplified equation using K- map are necessary.

The aforementioned step will allow us to know what kind of gates we need to use. This will lead us to know the ICs as well.

Although, using basic logic gates will lead us to some difficulties as well. The circuit will turn out to be more complicated as there will be more gates and many wires.

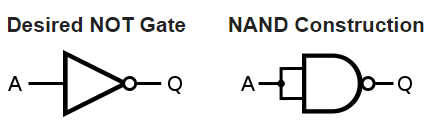
**Using Universal Gates:** Construction of the circuit using universal gates can be done using inverter “AND” and an inverter “OR” gates.

The truth table will give the simplified equation; and using K- map will give the specified gates which are needed.

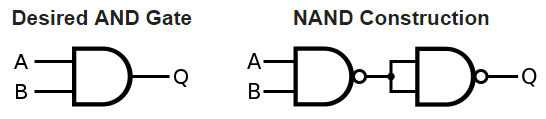
“AND”, “OR”, “NOT” and “XOR” gates can be made using “NAND” and “NOR” gates.

The implementation of the circuit in logisim will lead us to setup the circuit properly.

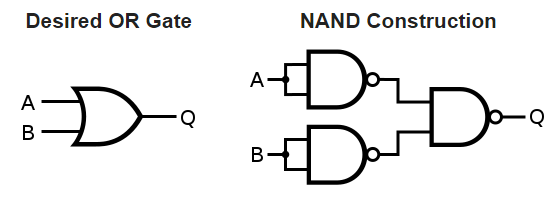
Basic gate implementation using NAND and NOR universal gate :



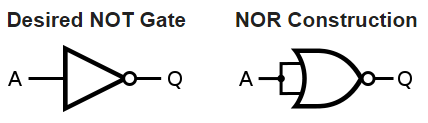
*Figure 1:* ***NOT*** *gate implementation using* ***NAND*** *gate.*

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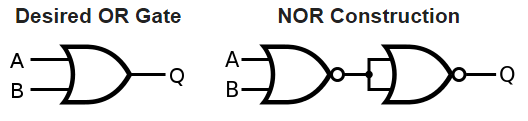
*Figure 2:* ***AND*** *gate implementation using* ***NAND*** *gate.*

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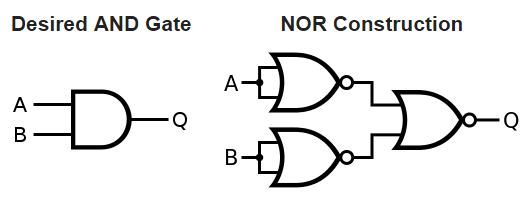
*Figure 3:* ***OR*** *implementation using* ***NAND*** *gate.*



*Figure 4:* ***NOT*** *gate implementation using* ***NOR*** *gate.*



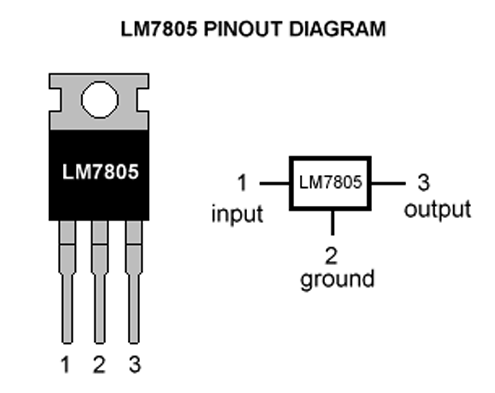
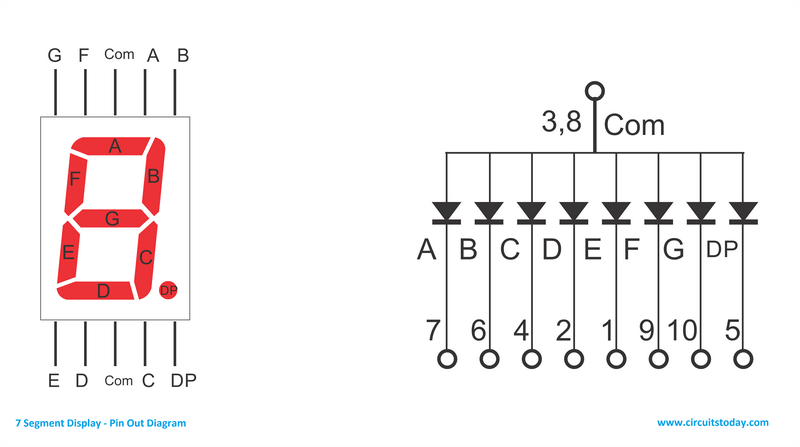
*Figure 5:* ***OR*** *gate implementation using* ***NOR*** *gate.*

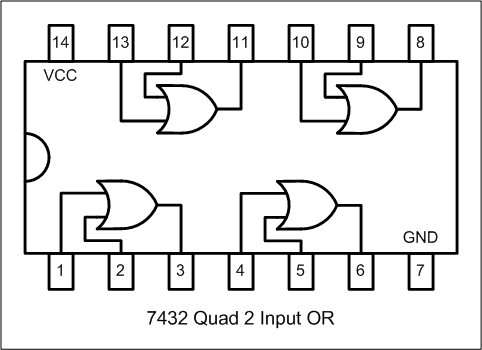


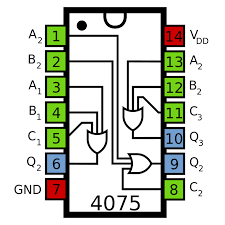
*Figure 6:* ***AND*** *gate implementation using* ***NOR*** *gate.*

**Using Multiplexer:**  To set up the circuit first we need to find the equations from the truth table. Four inputs are taken and three inputs are taken as select bits. The one other input left is used as high and low to find the equations.

1. **Equipment’s Pin Diagram**







**Figures: Pin Diagrams**

1. **Truth Table for the Combinational Circuit:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **KEY WORD** | **DECIMAL DIGIT** | **A** | **B** | **C** | a | B | c | d | e | f | g | **MINTERMS** |
| **C** | 0 | **0** | **0** | **0** | 1 | 0 | 0 | 1 | 1 | 1 | 0 | m 0 |
| **S** | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | m 1 |
| **E** | 2 | **0** | **0** | **1** | 1 | 0 | 1 | 1 | 0 | 1 | 1 | m 2 |
| **2** | 3 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | m 3 |
| **3** | 4 | **0** | **1** | **0** | 1 | 0 | 0 | 1 | 1 | 1 | 1 | m 4 |
| **1** | 5 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | m 5 |
| **-** | 6 | **0** | **1** | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 1 | m 6 |
| **6** | 7 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | m 7 |
|  | 8 | **1** | **0** | **0** | 0 | 1 | 1 | 0 | 0 | 0 | 0 | m 8 |
|  | 9 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | m 9 |

a = m0, m2, m4 e = m0, m4

b = m8 f = m0, m2, m4

c = m2, m8 g = m2, m4, m6

d = m0, m2, m4

1. **Hardware implementation in details:**

* We have eight letters in our project key word which are C, S, E, - and 6. For the combinational circuit part, we map these seven letters to binary input 0000 to 1111 and set output values a, b, c, d, e, f, g for the seven-segment display as required.
* For example, as we have used 3\*8 Decoder, ABC are select bits. We associate binary input 000 with the letter **C** and set the outputs as a, d, e, f, g in high of Seven segment display. The rest of the letters are associated in the same way.

001 for ‘**S**’= set the outputs **a, c, d, f, g** in high.

010 for ‘**E**’= set the outputs **a, d, e, f, g** in high.

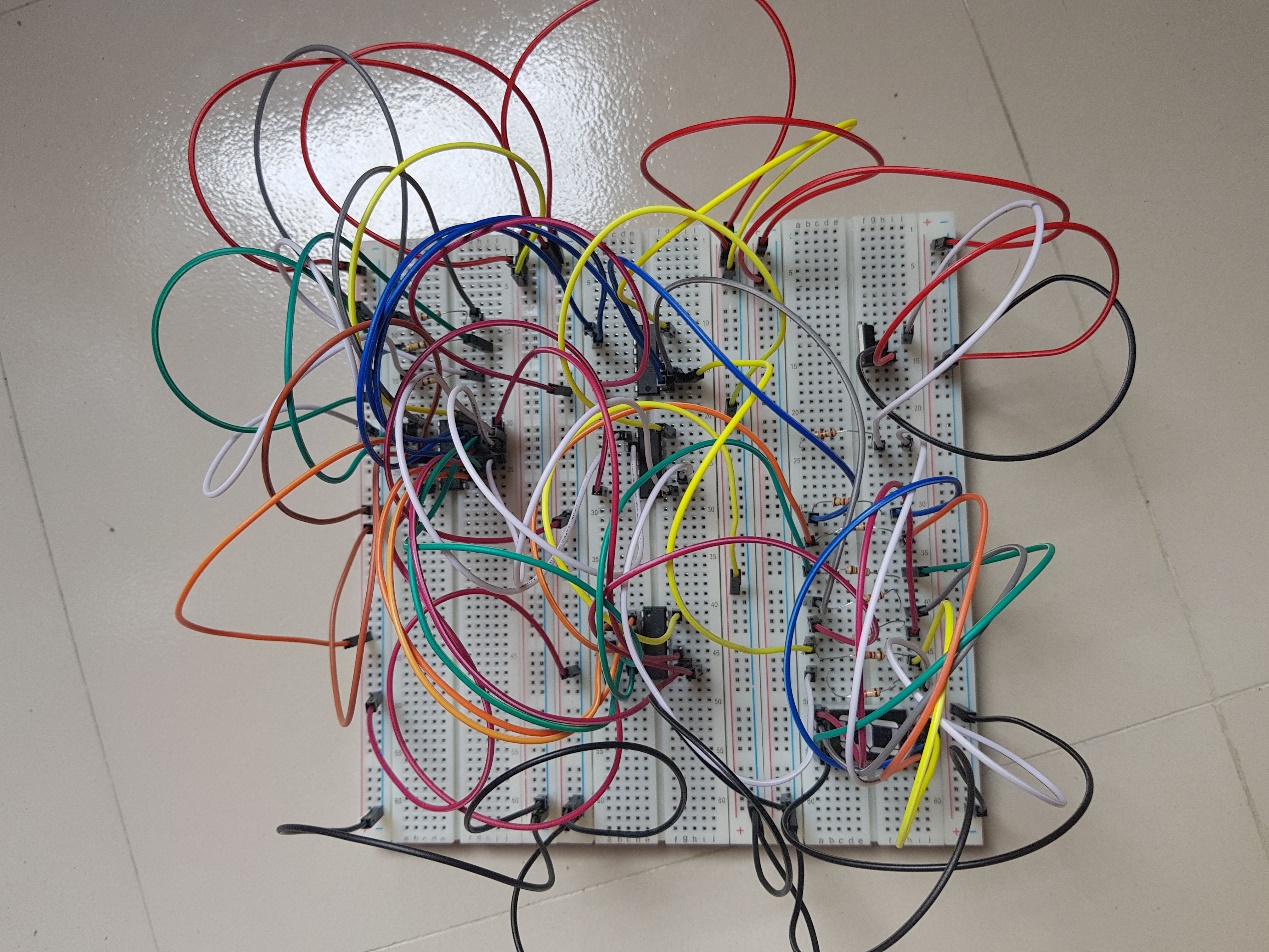
110 for ‘**–** ‘= set the outputs **g** in high.

101 for ‘6’= set the outputs **b, c** in high.

* Then we set the whole circuit using our required equipment’s according to IC pin diagram and logisim circuit diagram.

* We have used 3\*8 Decoder and some OR gates 7832 IC & 4075IC.
* We have used a voltage regulator that supplies 5 volt into the whole circuit so that our IC doesn’t get destroyed.

1. **Circuit Implemented Picture:**

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1. **Acknowledgement:**

The whole project of building a 7- segment display using a Decoder took us around 6-7 days to build. During this period of time, we not only knew the theory but also had some understandings on how to implement it practically. On top of that, we also gathered basic knowledge of other ways to implement the circuit.

The construction of the circuit would not be possible without the help of **Sanjida Islam** (lab instructor), who helped us on some of the obstacles we faced while setting up the circuit.

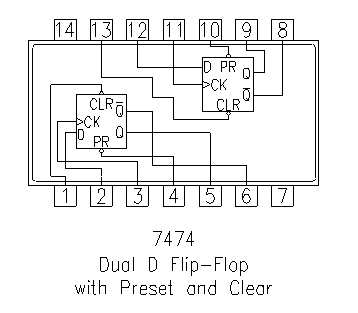
**Sequential Part**

**Required Components :**

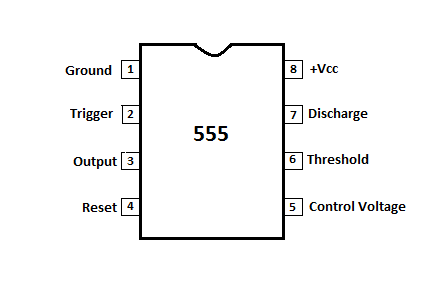
1. IC 74HC138P Decoder – 1 piece
2. IC 7474 D Flip-Flop-2 Piece
3. IC 7408 AND-3 Piece
4. IC 7432 OR-2 Piece
5. NE555 Timer- 1Piece
6. Capacitor-10uF{2 Piece}
7. Battery
8. Breadboard
9. Wires
10. Seven Segment Display (Common Cathode)
11. 1 KΩ Resistors - 6 piece,100 KΩ Resistor(2 Piece)

**Equipment Pin Diagram**

**Pin diagram of D-flip flop**



**Pin diagram of 555 timer**



**State Table-**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Code** | **Minterm** | **Present State**  A B C | **Next State**  A B C | **D Flip-Flop**  DA DB DC |
| C | m0 | 0 0 0 | 0 0 1 | 0 0 1 |
| S | m1 | 0 0 1 | 0 1 0 | 0 1 0 |
| E | m2 | 0 1 0 | 0 1 1 | 0 1 1 |
| - | m3 | 0 1 1 | 1 0 0 | 1 0 0 |
| 6 | m4 | 1 0 0 | 1 0 1 | 1 0 1 |
|  | m5 | 1 0 1 | X X X | X X X |
|  | m6 | 1 1 0 | X X X | X X X |
|  | m7 | 1 1 1 | X X X | X X X |

**K-Map For Flip-Flop:-**

**DA:-**

|  |  |  |  |
| --- | --- | --- | --- |
| 0  m0 | 0  m1 | 1  m3 | 0  m2 |
| 1  m4 | 1  m5 | X  m7 | X  m6 |

**DA=** BC+AB’

**DB:-**

|  |  |  |  |
| --- | --- | --- | --- |
| 1  m0 | 1  m1 | 1  m3 | 1  m2 |
| 0  m4 | 0  m5 | X  m7 | X  m6 |

**DB =** B’C+A’C’B

**DC:-**

|  |  |  |  |
| --- | --- | --- | --- |
| 1  m0 | 1  m1 | 0  m3 | 1  m2 |
| 0  m4 | 0  m5 | X  m7 | X  m6 |

**DC = AB’+A’C’**

**Final Circuit Diagram-**

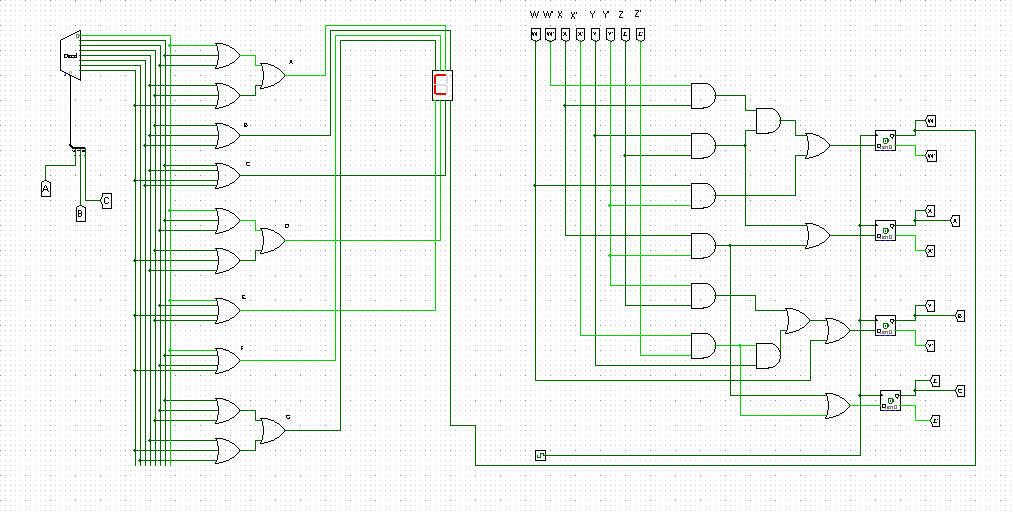
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Figure: logisim for Sequential and Combinational

**Discussion**

The project was to design a 7 segment display showing the word “**CSE - 6**”. At first we did the combinational circuit using K-Map. Then we did simulation using Logisim. At first we tired simulating using Multiplexer but the circuits were huge so we changed it and used Decoder. We couldn’t use NAND Gates or NOR Gates as we were instructed. Then we implemented the circuit. In implementing we faced some problem. Even though we connected them correctly but the output didn’t match. So we re-did everything and this time we got the desired output. The next step was the sequential part. This was the most curtail part of the circuit. First we did the state table and then used K-Map for the equations that we have to plot into the D-Flip flop to construct the circuit. We simulated the circuit using logisim. Here we were use 7-segment display to complete the project as instructed.